REMARKS

In response to the Final Office Action mailed June 16, 2003, Claims 1-5 and 7-20 were examined and rejected. Applicants amend Claims 1 and 11. Applicants reserve the right to prosecute the former claims in a divisional or continuation application. Applicants respectfully request reconsideration of pending Claims 1-5 and 7-20, as amended, in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejected claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,599,734 issued to Byun, et al. ("Byun") in view of Kroner, et al. (IEEE 2000) ("Kroner"). Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP 2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Claim 1

Applicants have amended Claim 1 to include the following:

> forming a SOG layer containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate. [Emphasis added]

Applicants respectfully submit that these features of Claim 1 are neither taught nor suggested by either Byun or Kroner. Namely, according to Byun,

> A disposable layer **24** having a first conductivity type impurity and a second conductivity impurity of a higher concentration than that of the first conductivity impurity is formed over the entire surface of the substrate by CVD process, as shown in FIG. **2**B, and then the resultant structure is subjected to an anneal treatment such as rapid thermal annealing or furnace so that a highly doped source/drain area of a shallow junction can be formed (FIG. **2**C). (Col. 3, lines 33-40) [Emphasis added]

As such, Byun fails to teach an SOG layer containing either an n-type impurity, or a p-type impurity, but not both, as required by Claim 1. The teachings of Byun are limited to a disposable layer comprised of a BPSG layer having both a p–type and an n-type impurity to a diffusion source. As is well known in the art, a p-type impurity refers to B or In, and an n-type impurity refers to P, As or Sb.

Furthermore, as correctly pointed out by the Examiner, Byun fails to provide any teachings or suggestions with regards to the additional implanting of impurity ions into the SOG layer by a plasma ion implantation method. However, according to the Examiner,

> It would have been obvious to one of ordinary skill in the art of making a semiconductor devices to incorporate Kroner's teachings into Byun's method to implant impurity ions into the SOG layer by a plasma ion implantation method to increase the concentration impurities in the SOG layer using a plasma ion implanter including an Ion Shower Implanter (ISI) because it is a doping method for high dose and low energy implants.

Applicants respectfully disagree with the Examiner's contention.

In fact, Applicants respectfully submit that the teachings of Kroner are limited to Ion Shower implanting for polydoping, as illustrated by FIG. 4 of Kroner. Specifically, Kroner describes:

> The use of high dose phosphorus ion shower implants to replace gas phase polysilicon doping was tested. . . . Polysilicon is desposited over the structured field oxide. If the polysilicon is doped by phosphine-oxygen phosphorus glass deposition, a fast diffusing arsenic species evolves and lowers the threshold voltage of the field oxide transistor, as shown in FIG. 5. If the polysilicon is doped by either conventional ion implantation or ion shower implant, the fast diffusing arsenic species does not show up. (*See* pg. 477, col. 2, paragraph 3.)

In contrast, claim 1, as amended, requires:

> additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate by a plasma ion implantation method to increase the concentration of impurities in the SOG layer. [Emphasis added]

Accordingly, even assuming that one skilled in the art modified Byun in view of Kroner, Applicants respectfully submit that the modification would require replacement of a disposable layer 24 with a deposition of polysilicon on the entire surface of substrate 21. Applicants respectfully submit that Kroner does not provide any teaching regarding Ion Shower implantation into an SOG layer.

As a result, the modification proposed by the Examiner fails to teach forming of an SOG layer as required by Claim 1. Further, the modification would fail to teach additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate by a plasma ion implantation method to increase the concentration of impurities in the SOG layer, as required by amended Claim 1. Moreover, Applicants submit that one skilled in the art would not modify Byun in view of Kroner since the BPSG layer of Byun is a dielectric while the doped polysilicon layer of Kroner is a semiconductor.

Accordingly, Applicants respectfully submit that the Examiner cannot establish a *prima facie* rejection of Claim 1, since the references of record fail to teach or suggest all the claim limitations and, specifically, the additional impurity implantation into portions of the SOG layer. Consequently, Applicants respectfully request that the Examiner allows Claim 1.

Claims 2-10

Claims 2-10 depend from Claim 1 and, therefore, include the patentable claim limitations of Claim 1, as described above. Consequently, Claims 2-10 are patentable over the references of record. Therefore, Applicants respectfully request that the Examiner allow Claims 2-10.

Claim 11

Claim 11 includes the following features, which are neither taught nor suggested by either Byun or Kroner:

> diffusing the impurity ions contained in the SOG layer into the semiconductor substrate by a solid phase diffusion method to form shallow junctions having a LDD region self-aligned underneath both sidewalls of the gate pattern and a highly doped source/drain region adjacent to the LDD region.

In contrast, Claim 1 of Byun includes the following limitation:

> forming a source and drain area of the second conductivity-type impurity on the substrate by diffusing the second conductivity type impurity of the disposable layer into the substrate by means of an annealing process. [Emphasis added]

In other words, based on the passage cited above (see col. 3, lines 33-40) and the limitation of Claim 1 of Byun, the resultant shallow junctions formed, according to Byun, consist of the second conductivity type impurity which has a higher concentration than that of the first conductivity impurity to form a highly doped source/drain area. In contrast, the diffusion of impurity ions, according to Claim 11, allows the formation of shallow junctions including lightly doped regions 28B, as well as a highly doped region 28A, as depicted in FIG. 8. This feature is neither taught nor suggested by Byun or Kroner or the references of record.

In other words, Byun is limited to the formation of a source/drain area of the second conductivity impurity type. In contrast, Claim 11, as amended, requires the formation of shallow junctions having the LDD region and a highly doped source/drain region. Furthermore, Byun fails to teach an SOG layer containing either an n-type impurity, or a p-type impurity, but not both, as required by Claim 11.

Therefore, Applicants respectfully submit that the Examiner cannot establish a *prima facie* rejection of Claim 11, since the combination of Byun in view of Kroner, as well as the references of record, fails to teach each of the claim limitations of Claim 11 and, specifically, the formation of shallow junctions having an LDD region and a highly doped source/drain region. Consequently, Applicants respectfully request that the Examiner allow Claim 11.

Claims 12-20

Furthermore, Claims 12-20 depend from Claim 11 and, therefore, include the patentable claim limitations of Claim 11. As a result, Claims 12-20 are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 12-20.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-5 and 7-20 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: September 10, 2003

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail , with sufficient postage, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 10, 2003

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Marilyn Bass September 10, 2003